REMARKS

Applicants amend claims 1-4, 6 and 8 and add new claim 9. Hence, claims 1-9 are all the claims pending in the application.

Claim rejections under 35 U.S.C. § 102

Claims 1-3 and 5-8 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Shigeta et al. (US Patent No. 6, 646, 625, hereinafter "Shigeta"). Applicants traverse the rejections at least for the following reasons.

Independent claims 1

Claim 1 recites, *inter alia*, said gamma correction memory delivering one of the plurality of K-bit output grayscale levels to said display device when said N-bit output video signal of said bit rate converter corresponds to one of the plurality of N-bit input grayscale levels."

In the rejection of claim 1, the Examiner alleges that Shigeta discloses the above-noted features of the invention as defined by claim 1. Applicants respectfully disagree.

Shigeta is directed to a method for driving a plasma display panel which includes a data converter 30 that converts a pixel data D into a converted pixel data HD (FIG. 6). Shigeta discloses a data converter that includes an ABL (automatic brightness control) circuit 31, a first data conversion block 32, a multi-level gray scale processing block 33 and a second data conversion block 34. Shigeta discloses that the conversion of the pixel data D into converted pixel data HD comprises the following steps.

However, Applicants respectfully submit that Shigeta does not disclose a gamma correction memory delivering one of the plurality of K-bit output grayscale levels to a display

device when a N-bit output video signal of a bit rate converter corresponds to one of the plurality of N-bit input grayscale levels. In particular, Shigeta discloses a method that receives an input pixel data D and converts the data into brightness tuning pixel Dbl. Inverse Gamma compensation is applied to the brightness tuning pixel Dbl and an average brightness data generated using the inverse Gamma compensation is supplied back to level tuning circuit through feedback (column 10, lines 20-34). Shigeta discloses that the multi-grayscale level processing unit 330 (alleged bit rate converter) is positioned after the inverse Gamma compensation of the bright tuning pixel data that takes place in the ABL 31 (FIG. 6), and thus, it would be illogical to deliver one of the plurality of K-bit output grayscale levels to a display device when a N-bit output video signal of a bit rate converter corresponds to one of the plurality of N-bit input grayscale levels.

With respect to the Examiners assertion that memory 4 (FIG. 2) corresponds to a gamma correction memory, Applicants submit that Shigeta discloses that memory 4 performs reading and writing the converted pixel data HD in accordance with the drive signal supplied by the drive control circuit (column 6, lines 18-26). However, Shigeta does not disclose a gamma correction memory in which a plurality of N-bit grayscale levels are **mapped** to a plurality of K-bit output grayscale level.

In addition, the Examiner asserts that Shigeta allegedly discloses "said gamma correction memory delivering one of the plurality of K-bit output grayscale levels to said display device when said N-bit output video signal of said bit rate converter corresponds to one of the plurality

of N-bit input grayscale levels" in FIG. 20 and column 16, lines 12-70. Applicants respectfully disagree.

Applicants submit that Shigeta discloses the relationship between input pixel data D and display brightness level in the drive modes A and B (FIG. 20, column 16, lines 12-16). Furthermore, Shigeta discloses that the input pixel data D maybe inverse-gamma corrected by setting the ratio of the number of times a light-emission in the light-emission sustaining step Ic of each sub-field to the inverse gamma ratio (column 16, lines 43-46). However, Shigeta does not disclose a gamma correction memory delivering one of the plurality of K-bit output grayscale levels to a display device when a N-bit output video signal of said bit rate converter corresponds to one of the plurality of N-bit input grayscale levels.

In view of the above, Applicants respectfully submit that claim 1 patentable over Shigeta and requests the Examiner to withdraw the rejection of claim 1 under 35 U.S.C. § 102(e).

With respect to dependent claim 6 which recites, *inter alia*, a first adder for adding a binary-1 to the least significant bit position of higher N bits of the M-bit input video signal, the Examiner contends Shigeta discloses the above-described feature. Applicants respectfully disagree.

Shigeta discloses an adder 342 (alleged fist adder) that adds the outputs of three scale multiplexers (339, 340 and 341). Inputs to all three of the scale multiplexers arrive from adder 332, which has the Error data (lower 2 bits of the converted pixel data HDp) as one of its input. The display data (upper 6 bits of the converted pixel data HDp) is only added with the carry out signal (Co) generated by the adder 332 and output to the dither processing unit. However,

Shigeta does not disclose a first adder for adding a **binary-1** to the least significant bit position of higher N bits of the M-bit input video signal. Therefore, Applicants respectfully submit that claim 6 should be allowable at least for the reason given above.

Claims 2, 3 and 5-8

Claims 2, 3 and 5-8 depend from claim 1, and therefore they are allowable by virtue of their dependency.

Claim rejections under 35 U.S.C. § 103

Claim 4 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shigeta in view of Lee et al. (US Patent No. 7,030,846, hereinafter "Lee"). Applicants traverse the rejection for the following reasons.

Applicants submit that Lee does not cure the deficient teachings of Shigeta, noted above with respect to claim 1. Furthermore, claim 4 depends from claim 1 which has been shown to contain allowable subject matter. Therefore, Applicants respectfully submit that claim 4 is allowable at least by virtue of their dependency and additional reasons given above.

New claim

Applicants respectfully submit that claim 9 recites, *inter alia*, a first adder for adding a binary-1 to the least significant bit position of higher N bits of the M-bit input video signal, and therefore, is allowable at least for the reason given above with respect to claim 6.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

#40,766

Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
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